I claim:

1. A method for adapting/tuning signal transit times on line systems or networks between integrated circuits which are mounted on printed circuit boards, which comprises:

providing printed circuit boards having capacitive load structures disposed on at least one conductor track path of a line system or network and disposed adjacent a location selected from the group consisting of a housing of an integrated circuit and housings of integrated circuits;

measuring all relevant delay or signal transit times on the line system or network between the integrated circuits;

selectively disconnecting specific ones of the capacitive load structures from the at least one conductor track path depending on the measured delay or signal transit times, in order to minimize maximum signal delays which occur.

2. The method according to claim 1, which comprises repeating the measuring step and the selectively disconnecting step.

3. The method according to claim 1, which comprises providing the capacitive load structures with a capacitance in a femtofarad range.

4. The method according to claim 1, which comprises providing the capacitive load structures with a capacitance in a sub-femtofarad range.

5. The method according to claim 1, which comprises performing the step of selectively disconnecting the capacitive load structures by laser cutting.

6. The method according to claim 1, which comprises providing the integrated circuits as high-speed memory modules on the printed circuit boards.

7. The method according to claim 1, which comprises adapting the signal transit times on the line systems or the networks between high-speed DRAM memory modules mounted on the printed circuit boards.

8. The method according to claim 7, which comprises not tuning chips and housings.

9. The method according to claim 8, which comprises providing the DRAM memory modules with different materials.

10. The method according to claim 9, which comprises tuning chips and housings differently.

11. The method according to claim 10, which comprises providing the DRAM memory modules with different materials.

12. The method according to claim 7, which comprises providing the DRAM memory modules with different materials.

13. The method according to claim 7, which comprises compensating manufacturing tolerances of the printed circuit boards.

14. The method according to claim 13, which comprises compensating manufacturing tolerances of chip housings.

15. The method according to claim 7, which comprises compensating manufacturing tolerances of chip housings.

16. A configuration for adapting/tuning signal transit times on line systems or networks between integrated circuits which are mounted on printed circuit boards, the device comprising:

a securing device for securing at least one printed circuit board having integrated circuits and having capacitive load structures disposed on at least one conductor track path of a line system or network adjacent a location selected from the group consisting of a housing of one of the integrated circuits and housings of the integrated circuits;

a measuring device for measuring relevant delay or signal transit times on the line system or the network between the integrated circuits on the at least one printed circuit board; and

a disconnection device for selectively disconnecting specific ones of the capacitive load structures in such a way that maximum delay times measured by the measuring device are minimized.

17. The configuration according to claim 16, comprising the at least one printed circuit board, the capacitive load structures having a form selected from the group consisting of surfaces and vias.

18. The configuration according to claim 17, wherein said disconnection device includes a cutting laser.

19. The configuration according to claim 16, wherein said disconnection device includes a cutting laser.

20. A memory module comprising:

a printed circuit board and at least one memory module mounted on it;

said printed circuit board including at least one conductor track forming part of a signal transmission network or line system which transmits signals to and from said memory module, said at least one conductor track having a region adjacent a housing footprint area of said memory module;

said printed circuit board having disconnectable line structures selected from the group consisting of surfaces and vias, said disconnectable line structures disposed at said region adjacent the housing footprint area of said memory module;

said disconnectable line structures forming capacitive load structures with respect to said at least one conductor track and a housing of said memory module when mounted;

certain ones said capacitive load structures being selectively disconnectable at conductor tracks with a maximum signal delay in order to minimize known maximum signal transit times.